CLAIMS

1. An interface circuit, comprising:

at least one microprocessor operable to perform one or more functions, said microprocessor including at least a time input terminal for receiving a time reference signal and a signal input terminal for receiving an input signal within a detectable microprocessor logic operating level;

at least one RS232 receiver having an input for receiving an AC voltage input signal and an output for transmitting a microprocessor logic operating voltage signal, the output of said at least one RS232 receiver being coupled to said signal input terminal of said at least one microprocessor; and

at least one time reference RS232 receiver having an input for receiving a constant time reference AC voltage signal and an output for transmitting a time reference voltage signal to said time input terminal of said at least one microprocessor.

2. The interface circuit of claim 1, further comprising a voltage divider coupled to said at least one time reference RS232 receiver to reduce the incoming operational voltage to within a detectable range.

3. The interface circuit of claim 1, further comprising a voltage divider coupled to said at least one RS232 receiver to reduce the incoming operational voltage to within a detectable range.

4. The interface circuit of claim 1, wherein the falling edge of the time reference signal is capable of interrupting said at least one microprocessor.

5. The interface circuit of claim 4, wherein during interruption of said at least one microprocessor, a reading is

taken at the input of said at least one RS232 receiver to determine if an external controller has been activated.

6. The interface circuit of claim 2, wherein said voltage divider is arranged such that said incoming operational voltage is between about zero to five volts.

7. The interface circuit of claim 2, wherein said voltage divider comprises a pair of resistors having predetermined values such that said incoming operational voltage is between about 0.5 to 2.7 volts.

8. The interface circuit of claim 2, further comprising an input logic high threshold voltage and an input logic low threshold voltage.

9. The interface circuit of claim 8, wherein said resistor values are set such that said incoming operational input logic high threshold voltage is between about 1.3 to 2.7 volts and said input logic low threshold voltage is between about 0.5 to 1.9 volts.

10. The interface circuit of claim 8, wherein said resistor values are set such that said incoming operational input logic high threshold voltage is about 2.1 volts.

11. The interface circuit of claim 8, wherein said resistor values are set such that said incoming operational logic low threshold voltage is about 1.1 volts.

12. The interface circuit of claim 1, further comprising at least twelve RS232 receivers.

13. The interface circuit of claim 1, wherein the output signal of said at least one RS232 receiver is coupled to at least one external controller.

14. The interface circuit of claim 13, wherein said at least one external controller is selected from a group comprising a thermostat, a switch, a relay contact, and a humidity controller.

15. The interface circuit of claim 1, further comprising a failsafe interface control circuit coupled between an output terminal of an external controller and said input of said at least one RS232 receiver, whereby said failsafe interface control circuit is capable of minimizing microprocessor malfunctioning.

16. A method for detecting an AC voltage input signal, comprising:

providing an interface circuit including at least two RS232 receivers, each RS232 receiver being coupled to an input of a microprocessor;

splitting a received input signal into a first and second signal, the first signal being coupled to a time reference circuit, said time reference circuit including one of said at least two RS232 receivers, the second signal being coupled to at least one external controller circuit, said external controller circuit including at least one of said at least two RS232 receivers;

detecting said first signal at said time reference circuit output;

interrupting said microprocessor; and

sampling the output of the at least one external controller circuit after a predetermined delay from interrupting the microprocessor.

17. The method of claim 16, further comprising a plurality of external controller circuits.

18. The method of claim 16, wherein, if a signal is detected during the sampling step, the method further comprises activating a controller circuit to perform a predetermined function.

19. The method of claim 18, wherein the predetermined function comprises activating a load circuit.

20. The method of claim 18, wherein the step of activating a controller circuit comprises activation of one of a relay, a switch or a driver circuit.